Course Code: ECE2015	**Course Title:** Computer Architecture	**TPC**	**4**	**0**	**4**
Version No.	**1.0**				
Course Pre-requisites/ Co-requisites	**ECE1003**				
anti-requisites (if any).	**None**				
Objectives:	1. To understand the structure, function and characteristics of computer systems along with number systems and arithmetic 2. To understand the design of the various functional units and components of computers with their significance 3. To identify the elements of modern instructions sets and their impact on processor design				
Expected Course Outcome:	On completion of the course, students will have the ability to 1. Apply different formats of data representation and number systems 2. Analyse various algorithms to perform any signed and unsigned arithmetic operations 3. Build assembly language programs for specific applications by understanding the fundamentals of microprocessor 4. Design the control unit and identify the importance of different types of control units 5. Outline the memory hierarchy, draw the importance of cache memory and construct the different types of cache mapping techniques 6. Describe the pipelined and parallel processors and their significance				

COs Mapping with POs and PEOs

	Course Outcome Statement	PO's / PEO's
CO1	Apply different formats of data representation and number systems.	PO1, PO2, PO3
CO2	Assemble a simple computer with hardware design including data format, instruction format, instruction set, addressing modes, and bus structure.	PO1, PO2, PO3
CO3	Understand the hierarchy of Memory and cache memory mapping techniques	PO1, PO2, PO3, PO5
CO4	Design and analyse Arithmetic/Logic unit, control unit, data, instruction and address flow.	PO1,PO2,PO3, PO5
CO5	Design simple assembly language programs that make appropriate use of a registers and memory.	PO1, PO2, PO3
		TOTAL HOURS OF INSTRUCTIONS: 60

Module No. 1	Computer Evolution & Arithmetic	12 Hours
Evolution of computers, Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance– Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Bus and Bus organization, Memory location and addresses.		
Module No. 2	ALU	12 Hours
Arithmetic: Integer Arithmetic, Addition and Subtraction of signed and unsigned numbers, Multiplication of signed and unsigned numbers, 2's Complement method for multiplication, Booths Algorithm, Hardware Implementation, Array Multiplier, Integer Division, Restoring and Non Restoring algorithms, Floating point operations.		
Module No. 3	I/O Organization	12 Hours
Microprocessors, Instruction format, Instruction set, Addressing modes. Assembly Language Programming, Stack, Subroutine, Interrupt, Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses, Interface Circuits, Standard I/O, Interfaces – PCI Bus, SCSI Bus, USB.		
Module No. 4	Central Processing Unit and parallel processing	12 Hours
Basic Processing Units: Fundamental concepts, Instruction Sequencing, Execution cycle, Hardwired control, Micro programmed control. Instruction level pipelining and Superscalar Processors, Multiple Processor Organizations, Closely and Loosely coupled multiprocessors systems, Symmetric Multiprocessors, Clusters, UMA NUMA, and Vector Computations.		
Module No. 5	Memory Organization	12 Hours
Memory Organization: Semiconductor memory technologies, hierarchy, Interleaving, Main Memory RAM and ROM chips, Address map, Associative memory-Hardware organization. Match logic. Cache memory-size vs. block size, Mapping functions-Associate, Direct, Set Associative mapping. Replacement algorithms, write policies. Auxiliary memory-Magnetic tapes etc.		
Text Books. 1. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson Education, Tenth Edition, 2016. 2. M. Morris Mano, Rajib Mall, Computer System Architecture, Pearson Education Third Edition,2017		
References 1. Carl Hamacher, Zvonkovranesic, Safwat Zaky , Computer Organization, McGraw Hill, Fifth Edition,2011.		
Mode of Evaluation	**Continuous Assessment Tests and Final Assessment Test-60%, Practical Assessment and practice tests-40%** Continuous Assessment Test-1 20% Continuous Assessment Test-2 20% Final Assessment Test 20% Practical Assessment (Mini Project) 20% Practice Tests 20%	