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Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE2015

Course Title: Computer Architecture

Set number: 2

Date of Exam: 16/05/2023 (AN)

Duration: 120 Min

Total Marks: 60 (B2)

Instructions: All questions are cumpolsory

Q1 Develop an 8086 Assembly Language Program (ALP) to find a number in an array of 27 numbers located at 2000H: 5000H. An optimum ALP is expected. **(15 M)**

Q2 Discuss the hardware and software interrupts of the 8086 microprocessor. **(15 M)**

Q3 What is task of the control unit? Discuss the microprogrammed control unit. **(15 M)**

Q4 Elaborate the significance of cache memory in recent computers. Perform the memory mapping between the Cache memory of 64 kB to the main memory of 8 GB using 4 way set associative method where the block or page or frame size is of 8 KB. Consider each memory location is byte addressable. Depict the mapping using suitable diagram. **(15 M)**

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	4	CO3	PO1, PO2, PO3			15
Q2	4	CO3	PO1, PO2, PO3, PO5			15
Q3	5	CO4	PO1, PO2, PO3, PO5			15
Q4	5	CO5	PO1, PO2, PO3, PO5			15

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Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE2015

Course Title: Computer Architecture

Set number: 3

Date of Exam: 16/05/2023 (FN) (B1)

Duration: 120 Min

Total Marks: 60

Instructions: All questions are cumpolsory

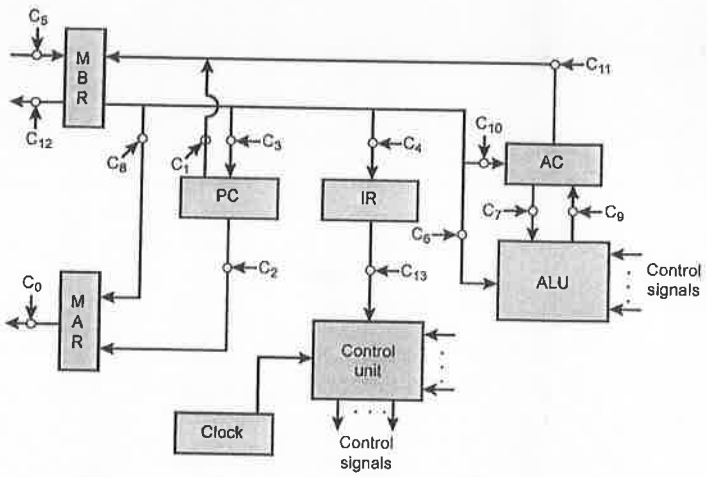
Q 1 Draw and discuss the flowchart to find the average of n 16-bit numbers using 8086 Assembly Language Program. **(15 M)**

Q 2 **(15 M)**

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00000	3C	22	10	38	6F	13	2C	2A	33	22	21	67	EE	F1	32	25
00010	11	3C	32	88	90	16	44	32	14	30	42	58	30	36	34	66
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00100	4A	33	3C	4A	AA	1A	1B	A2	2A	33	3C	4A	AA	1A	3E	77
00110	C1	58	4E	C1	4F	11	66	F4	C5	58	4E	20	4F	11	F0	F4
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00250	00	10	10	20	3F	26	33	3C	20	26	20	C1	3F	10	28	32
00260	20	4E	00	10	50	88	22	38	10	5A	38	10	4C	55	14	54
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
003E0	3A	10	45	2F	4E	33	6F	90	3A	44	37	43	3A	54	54	7F
003F0	22	3C	80	01	3C	4F	4E	88	22	3C	50	21	49	3F	F4	65

Using the above table find the physal address of the TYPE 42 interrupt of 8086 microprocessor.

Q 3



For the IAS computer instructions, LOAD100, ADD 200, STOR 300; derive the hardwire control unit using state table method. **(15 M)**

Q 4 What do you understand by cache memory mapping? Using suitable diagrams discuss different cache memory mapping. **(15 M)**

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	4	CO3	PO1, PO2, PO3			15
Q2	4	CO3	PO1, PO2, PO3, PO5			15
Q3	5	CO4	PO1, PO2, PO3, PO5			15
Q4	5	CO5	PO1, PO2, PO3, PO5			15