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Name of the Examination: WINTER 2022-2023 – CAT-2

Course Code: ECE2015 | **Course Title: Computer Architecture**

Set number: 2 | **Date of Exam: 28-03-2023** (AN)

Duration: 90 Min | **Total Marks: 50** (B_2)

Instructions: All questions are cumpolsory

Q1. Draw and discuscuss the hardware structure for addition and substration.

Q2. Discuss IEEE 32-bit floating point representation with an example.

Q3 Perform 9*3=27 using a suitable algorithm.

Q4. List the type of instruction set 8086 microprocessor have. Discuss each with two examples.

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	CO2	PO1, PO2, PO3			10
Q2	1	CO3	PO1, PO2, PO3, PO5			10
Q3	1	CO3	PO1, PO2, PO3, PO5			10
Q4	2	CO4	PO1, PO2, PO3, PO5			20

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Name of the Examination: WINTER 2022-2023 – CAT-2

Course Code: ECE2015 | **Course Title: Computer Architecture**

Set number: 3 | **Date of Exam: 28-03-2023** (FN)

Duration: 90 Min | **Total Marks: 50** (B1)

Instructions: All questions are cumpolsory

Q1 Perform the following using 2's complement: (-9)+(-8)=-17 and 8+8=16. Also discuss the advantages of 2's complement over the sign-magnitude representation.

Q2 Represent the 107.0125 in IEEE 32-bit floating point representation.

Q3 Perform 7/3 using restoring algorithm.

Q4. Discuss the memory segmentation of 8086 microprocessor.

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	CO2	PO1, PO2, PO3			20
Q2	1	CO3	PO1, PO2, PO3, PO5			10
Q3	1	CO3	PO1, PO2, PO3, PO5			10
Q4	2	CO4	PO1, PO2, PO3, PO5			10